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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/655,595	09/06/2000	William F. Beausoleil	POU9-2000-0045-US1	9321

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EXAMINER	
STEVENS, THOMAS H	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 11/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/655,595	BEAUSOLEIL ET AL.	
	Examiner	Art Unit	
	Thomas H. Stevens	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-5 were examined.

Section I: Non-Final Rejection (4th Office Action)

Specification

2. Pages 1 and 5, line 8 is missing application serial numbers. Correction is advises.

Claim Rejections - 35 USC § 103

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

Claims 1-5 are rejected under 35 U.S.C. 103 (a) as obvious by Donath ("Placement and Average Interconnection Lengths of Computer Logic" (1979) (hereafter, Donath) in view of Butts et al., (US Patent 5,452,231 (1995)) (hereafter Butts). Donath teaches a process to find the amount of space required for the interconnection governed by the total length of the wire to accommodate the spacing between wires (pg. 272, Introduction, left column) for pc boards, logic chips, cards, etc (pg. 272, Introduction, left column) but fails to teach simulation/emulation between pluralities of test circuit boards. Butts teaches interconnection of a hardware emulation with a circuit design in response to the input circuit information with at least two electronically reconfigurable logic assemblies (columns 86-87, lines 66-68 and 1-4, respectively); but doesn't teach wire length.

At the time of invention, it would have been obvious to one of ordinary skill in the art to integrate the two pieces of art to double the capacity to which doubling the number of transistors per chip (Butts: column 3, lines 40-45) to provide better upper

bound for significantly lower interconnection length between logic devices (Donath: abstract).

Per claims 1 and 5: emulation hardware logic with two printed circuit boards (Butts: columns 86-87, lines 66-68 and 1-4, respectively); interconnected multi-conductor cable (Donath: title; Butts: column 4, lines 35-40); determining cable length (Donath: pg. 272, right column 2nd paragraph); denote cable length (track requirements and results for placement of lengths: Donath: pg. 272, right column last paragraph to pg. 273, left column 1st paragraph); inputting a test pattern to the cable (Butts: column 21, lines 33-35); test pattern comprised of binary data (Butts: column 42, lines 25-32); collecting an output data pattern (Butts: columns 41-42, Configuration Section 1.4); compiling (Butts: column 75, line 40) emulation program to account for each pair of conductors (Butts: column 22, lines 37-39 with Donath: pg.273, left column, 2nd paragraph, lines 6-9), the emulation program corresponding to a logic design for an integrated circuit(columns 86-87, lines 66-68 and 1-4, respectively).

Per claim 2: test pattern is binary of alternating "1s" and "0s". (Butts: column 42, lines 25-32).

Per claims 3 and 4: where one cable length is denoted by having not interchanged pair of conductors (specification pg. 9, lines 6-7 states "swapping different pairs denote different lengths", thus different length is unique by way of design preference to which Donath states: Donath, Introduction, pg. 272).

Citation of Relevant Art

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- IBM. "Machine Organization and Rent's Rule" 1999.: teaches a method on interconnection wire length.

- US Patent 5,963,735A Sample et al.: teaches a system of physical emulation involving utilization of unused circuit paths in the logic gates.

Section II: Response to Arguments (2nd Office Action)

132/103 Rejections

7. Applicants are thanked for addressing this issue. Applicant's arguments, with respect to the previous office action, rejections to claims 1-5 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground of rejections is made, for one, in view of Butts et al. and Donath.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715, Monday-Friday (8:00 am- 4:30 pm EST).

If attempts to reach the examiner by telephone are unsuccessful, please contact examiner's supervisor Mr. Leo Picard ((571) 272-3749). The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.. Answers to questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) (toll-free (866-217-9197)).

October 27, 2005

TS

Paul L. Rodriguez 11/10/05

Primary Examiner
Art Unit 2125